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Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1.   (Currently Amended) A processor for use in a Voice-over-Internet Protocol telephone, including:

a Voice-over-Internet Protocol processor core operable to transmit computer data and voice data over a computer network;

a bus on which signals internal to the processor are routed;

memory coupled to the Voice-over-Internet Protocol processor core through the bus;

one or more communication ports coupled to the Voice-over-Internet Protocol processor core and memory through the bus; and

one or more IEEE 802.3 media access controllers (MACs) coupled to the Voice-over-Internet Protocol processor core through the bus,

wherein the Voice-over-Internet Protocol processor core transmits the computer data and the voice data through the one or more communication ports, and wherein the one or more communication ports and the one or more IEEE 802.3 MACs are integrated onto a same chip as the Voice-over-Internet Protocol processor core.

2.   (Currently Amended) The processor of claim 1, wherein the one or more communication ports are further include one or more pulse code modulation (PCM) ports.

3.   (Cancelled)

4.   (Currently Amended) The processor of claim 1, wherein the one or more communication ports ~~are~~ further include one or more universal serial bus (USB) ports.

5.   (Previously Presented) The processor of claim 1, wherein the one or more communication ports allow the Voice-over-Internet Protocol processor core to be coupled to one or more external components without external interfacing circuitry.

6.   (Currently Amended) An apparatus, comprising:
a single-chip Voice-over-Internet Protocol network processor operable to transmit computer data and voice data over a computer network, the single-chip Voice-over-Internet Protocol network processor including,
          a flexible peripheral interconnect (FPI) bus; ~~and~~
          one or more universal serial bus (USB) ports integrated onto the single chip through the FPI bus, the one or more USB ports operable to provide an interface between the Voice-over-Internet Protocol network processor and one or more USB compatible devices without having to provide external interfacing circuitry; and
          one or more IEEE media access controllers (MACs) integrated onto the single chip through the FPI bus.

7.   (Cancelled)

8.   (Currently Amended) The apparatus of claim 6 [[7]], wherein the single-chip Voice-over-Internet Protocol network processor further includes one or more pulse code modulation (PCM) ports integrated onto the single chip through the FPI bus.

9.   (Previously Presented) The apparatus of claim 8, wherein each PCM port is operable to handle up to 30 time slots, and wherein each time slot is capable of handling a 64K

bit/sec voice channel.

     10.   (Currently Amended) A system, comprising:

a single-chip Voice-over-Internet Protocol network processor operable to transmit
computer data and voice data over a computer network, the single-chip Voice-over-Internet
Protocol network processor including,

     a flexible peripheral interconnect (FPI) bus; ~~and~~

     one or more universal serial bus (USB) ports integrated onto the single chip
through the FPI bus, the one or more USB ports operable to provide an interface between
the Voice-over-Internet Protocol network processor and one or more USB compatible
devices without having to provide external interfacing circuitry;

     <u>one or more IEEE media access controllers (MACs) integrated onto the single</u>
<u>chip through the FPI bus;</u> and

a memory unit coupled to the Voice-over-Internet Protocol network processor, the
memory unit operable to store programs used by the Voice-over-Internet Protocol network
processor.

     11.   (Cancelled)

     12.   (Currently Amended) The system of claim <u>10</u> [[11]], wherein the single-chip
Voice-over-Internet Protocol network processor further includes one or more pulse code
modulation (PCM) ports integrated onto the single chip through the FPI bus.

     13.   (Previously Presented) The system of claim 12, wherein each PCM port is
operable to handle up to 30 time slots, and wherein each time slot is capable of handling a 64K
bit/sec voice channel.

14.   (Previously Presented) The system of claim 12, further comprising a digital-to-analog/analog-to-digital (DA/AD) converter connected to the single-chip Voice-over-Internet Protocol network processor through one of the one or more pulse code modulation (PCM) ports integrated onto the single chip.

15.   (Previously Presented) The system of claim 14, further comprising a microphone, a speaker, and a handset, each connected to the single-chip Voice-over-Internet Protocol network processor through the DA/AD converter.

16.   (Previously Presented) The system of claim 15, further comprising a keypad interfaced with the single-chip Voice-over-Internet Protocol network processor, the keypad operable to allow a user to dial telephone numbers.

17.   (Previously Presented) The system of claim 16, further comprising a liquid crystal display (LCD) operable to display information entered through the keypad.

18.   (New) The processor of claim 1, further comprising a repeater coupled to the Voice-over-Internet Protocol processor core through the bus, wherein the repeater is integrated onto the same chip as the Voice-over-Internet Protocol processor core.